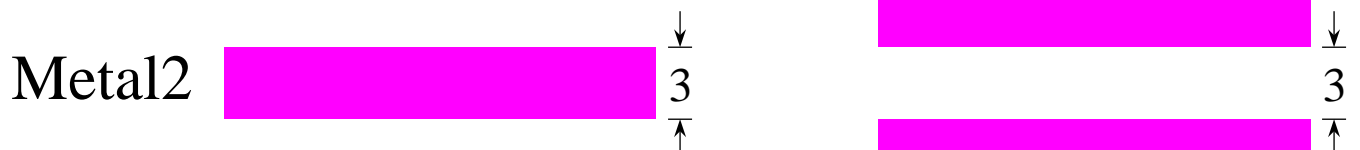
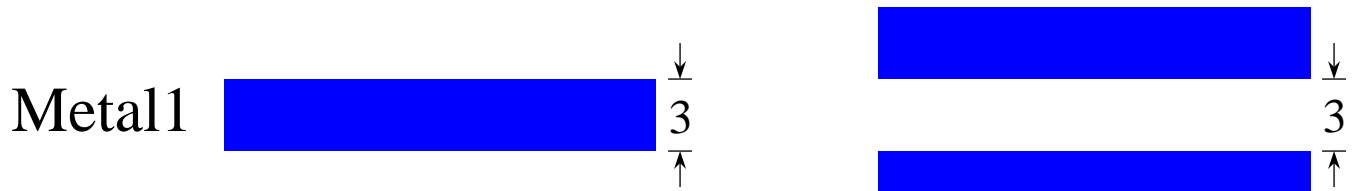
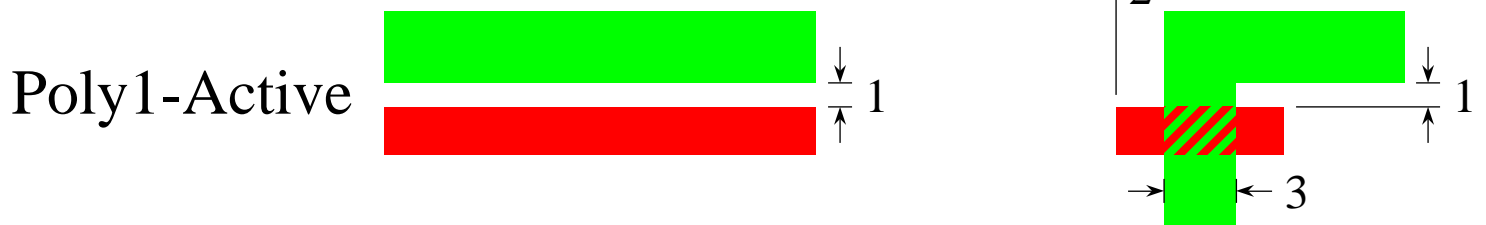
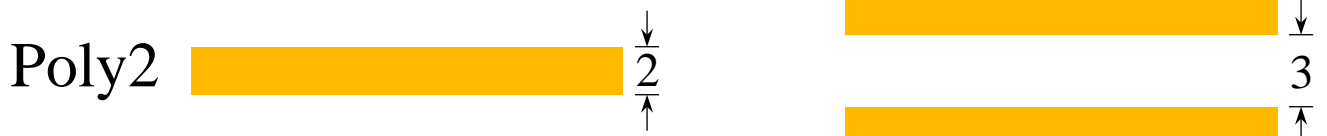
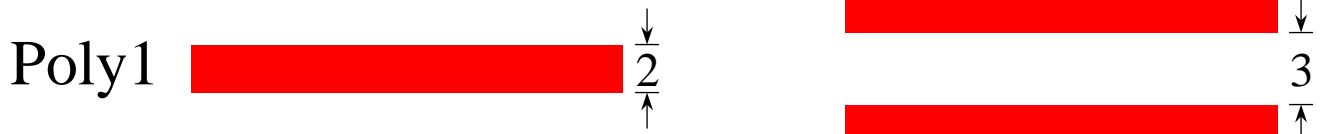
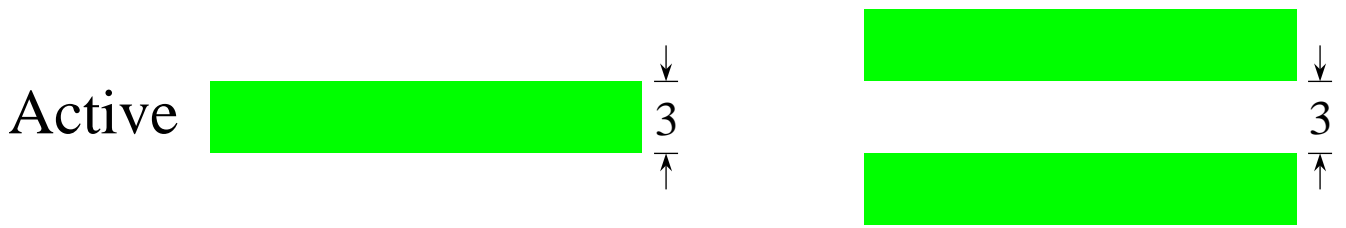


Layout for Analog Integrated Circuits

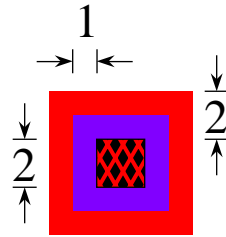
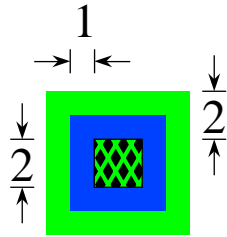
- ▶ **Layout** is the process of specifying the physical placement of and interconnections between all of the devices in a circuit.
- ▶ Layout is used to generate all of the mask layers used for chip fabrication.
- ▶ Layout for **digital** circuits:
 - Usually many transistors
 - Many transistors are minimum size
 - Transistors are sized to minimize delays
 - Focus on interconnections between modules
- ▶ Layout for **analog** circuits:
 - Usually relatively few transistors
 - Few transistors are minimum size
 - Transistors are sized to minimize offsets
 - Focus on optimizing individual devices

Common **SCMOS** Design Rules

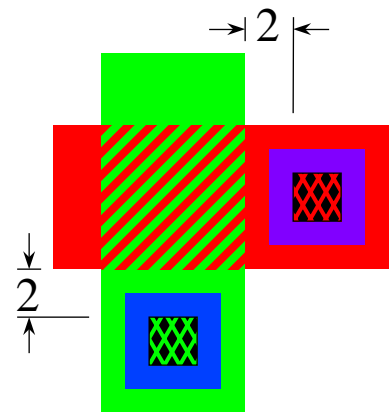
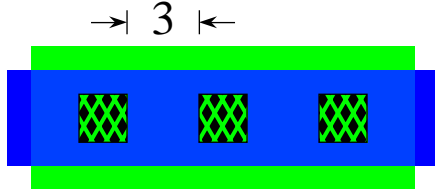


Common **SCMOS** Design Rules

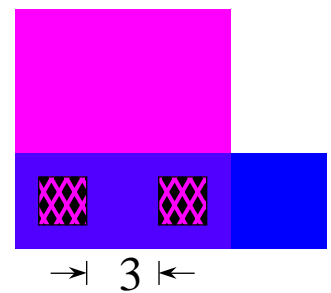
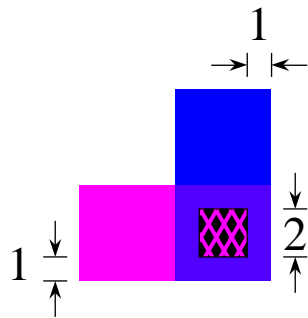
Contacts



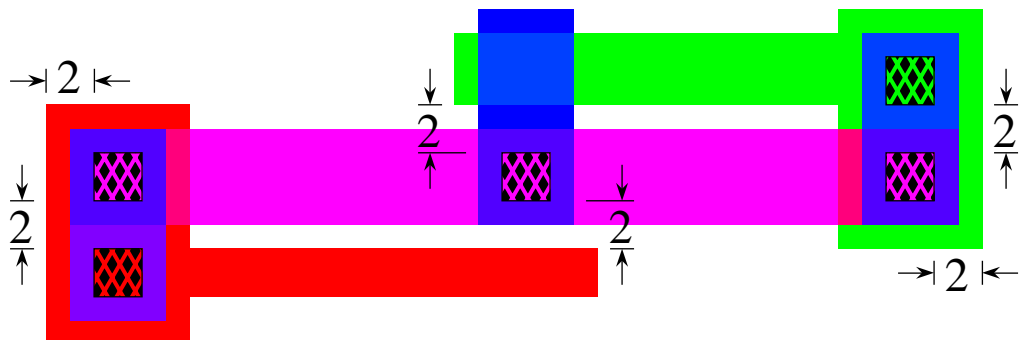
Contact Spacing



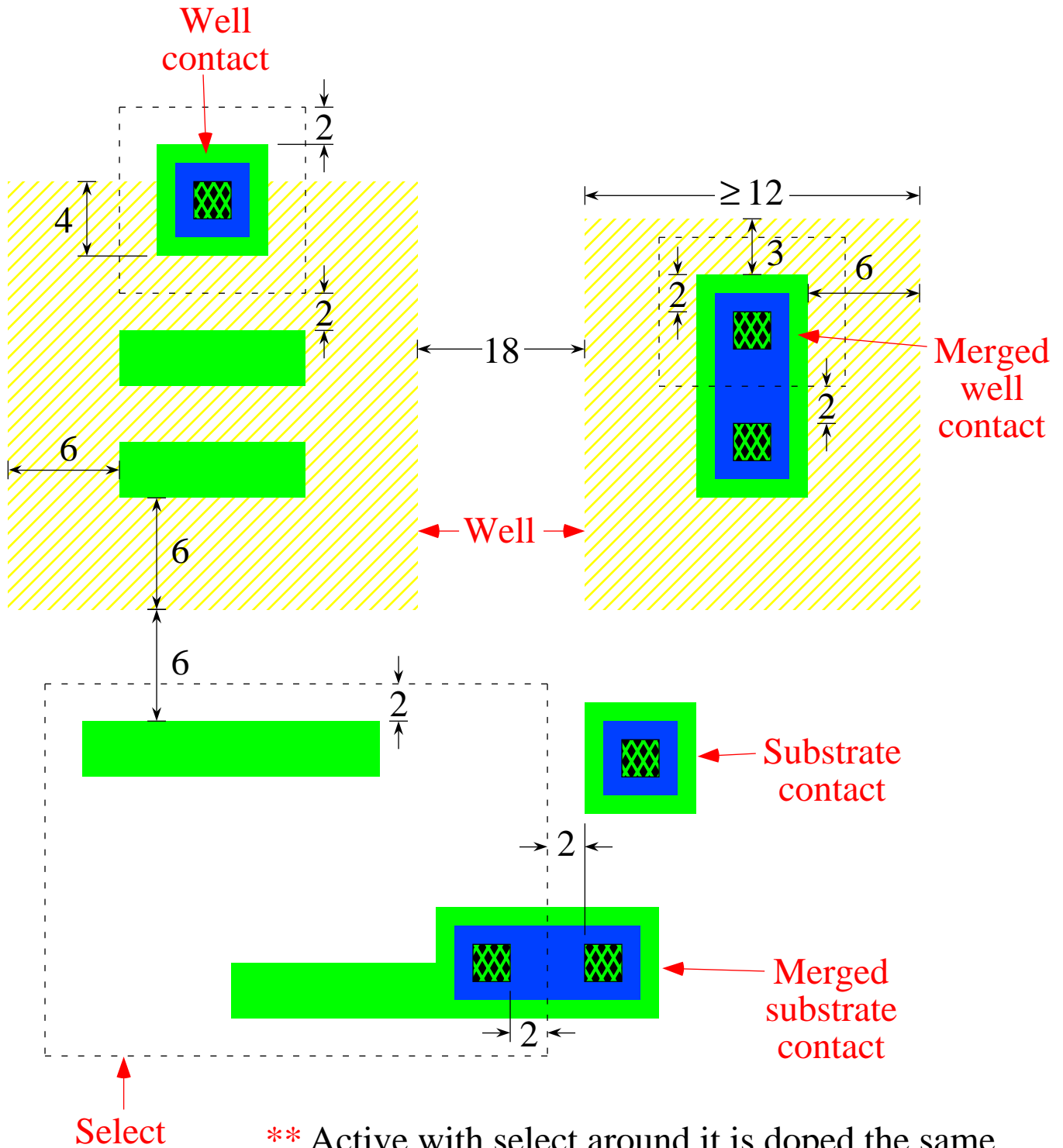
Vias



Via Spacing

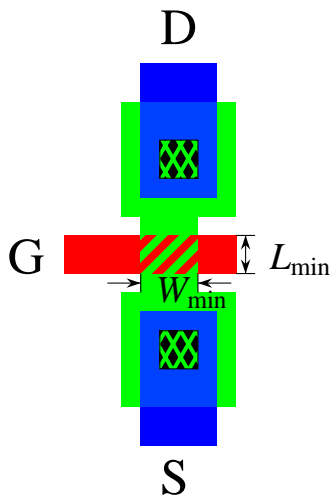


Common **SCMOS** Design Rules

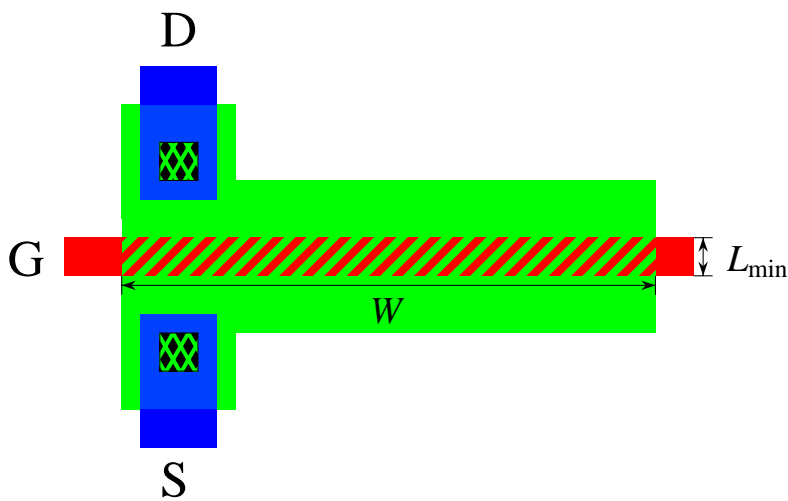


** Active with select around it is doped the same type as the well. Active without select is doped the same type as the substrate.

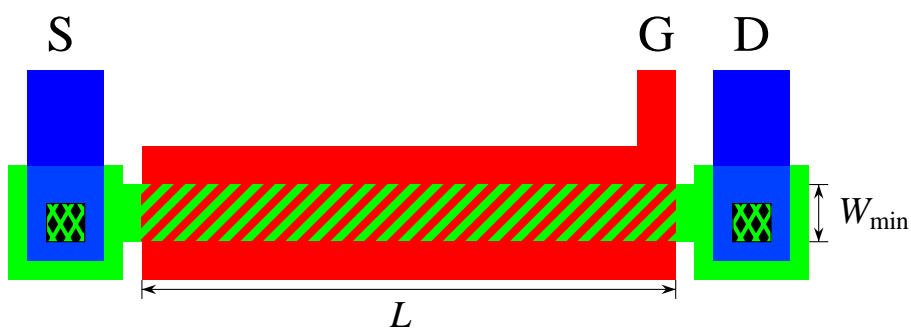
MOS Transistor Layout



Minimum size
 W_{min} and L_{min} set by design rules

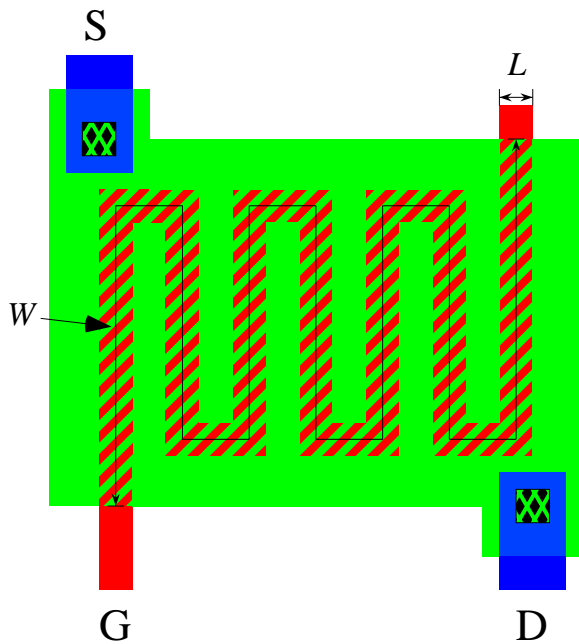


Wide
Strong
Large W/L

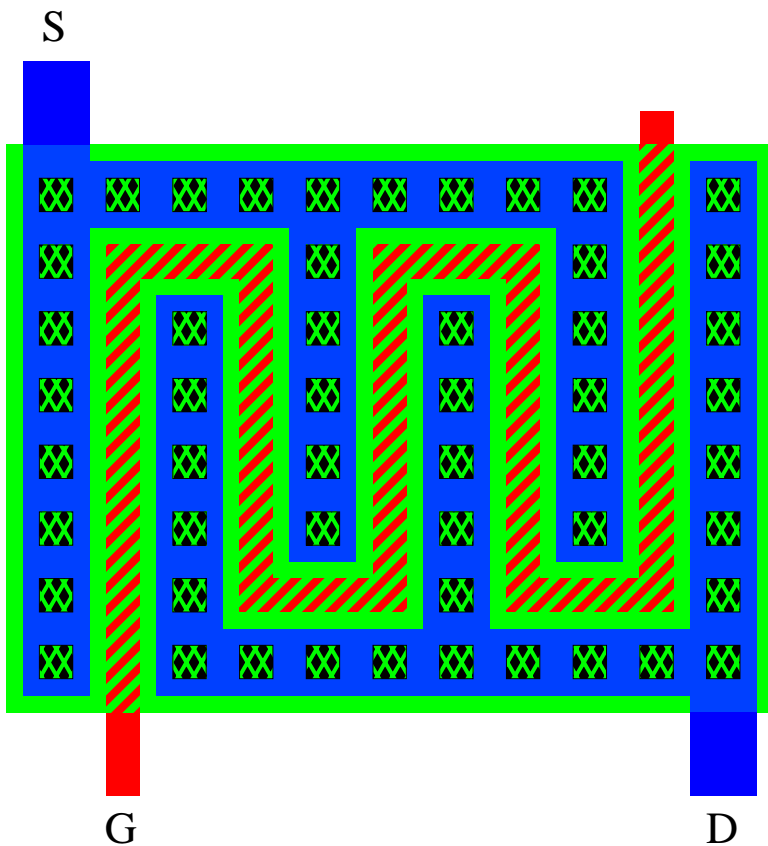


Long
Weak
Small W/L

Very Wide MOS Transistors: Serpentine Transistors

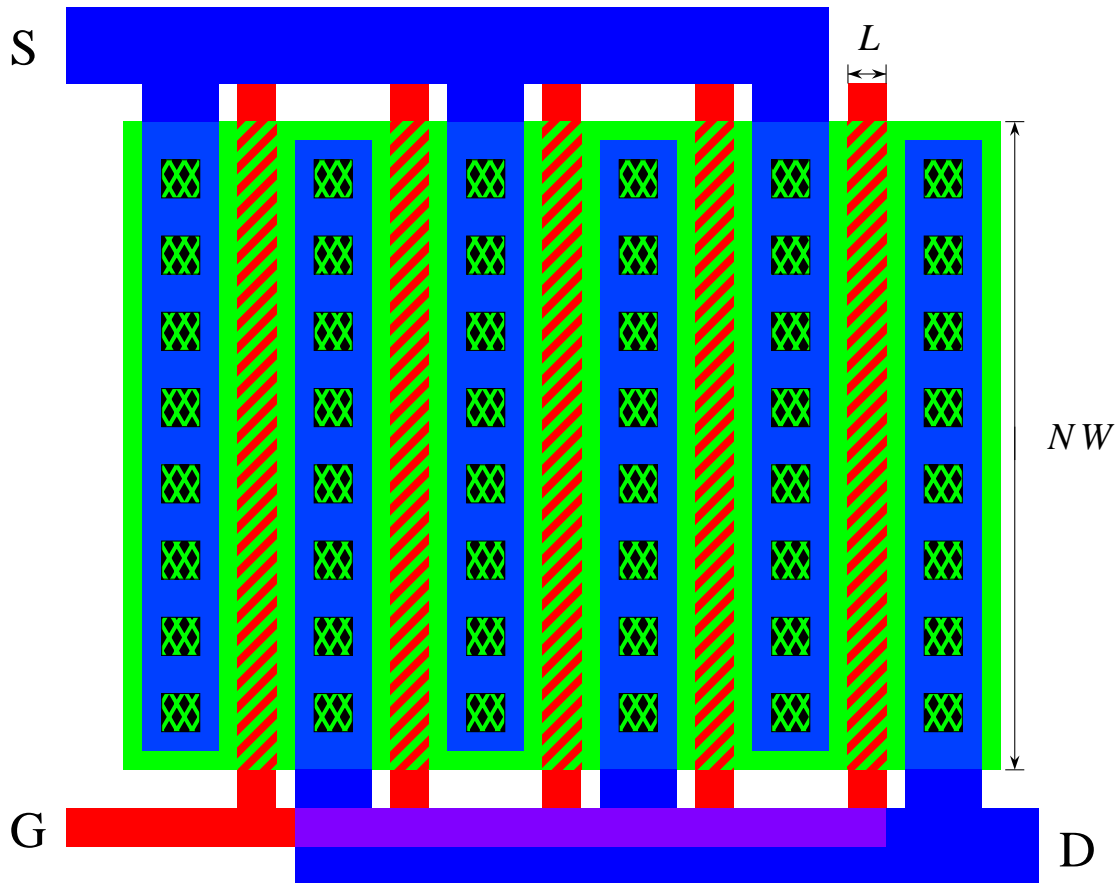


$W \gg L$
Source and drain
are interdigitated



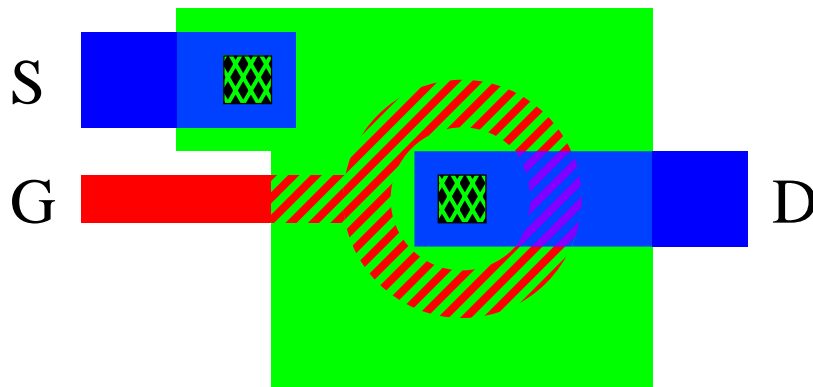
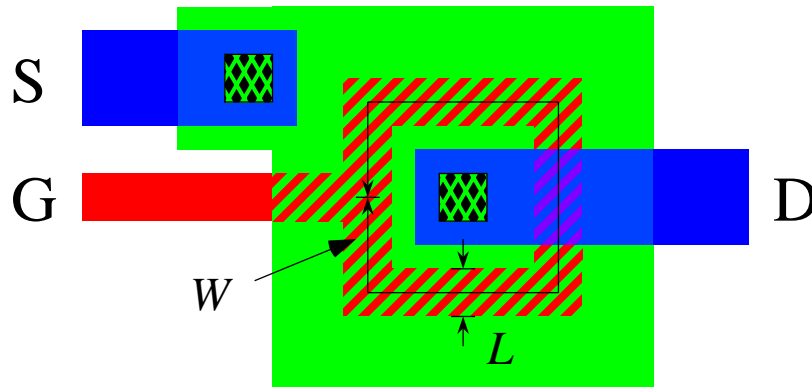
Minimize source
and drain series
resistance by using
many contacts

Very Wide MOS Transistors: Stacked Transistors



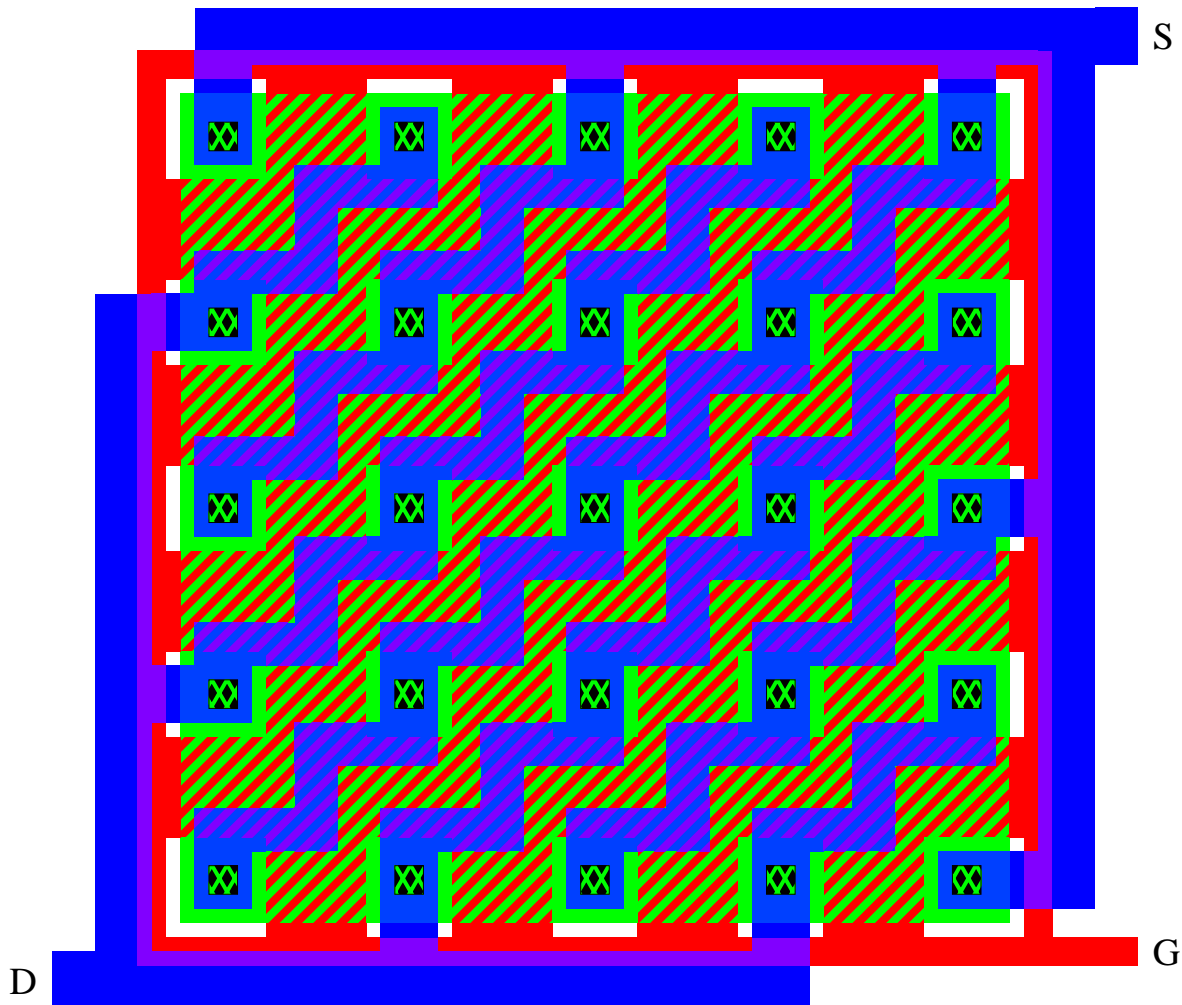
- ▶ Similar to serpentine transistors, but no bends.
- ▶ Source/drain regions shared \Rightarrow reduced C_S and C_D .

Very Wide MOS Transistors: Ring Transistors



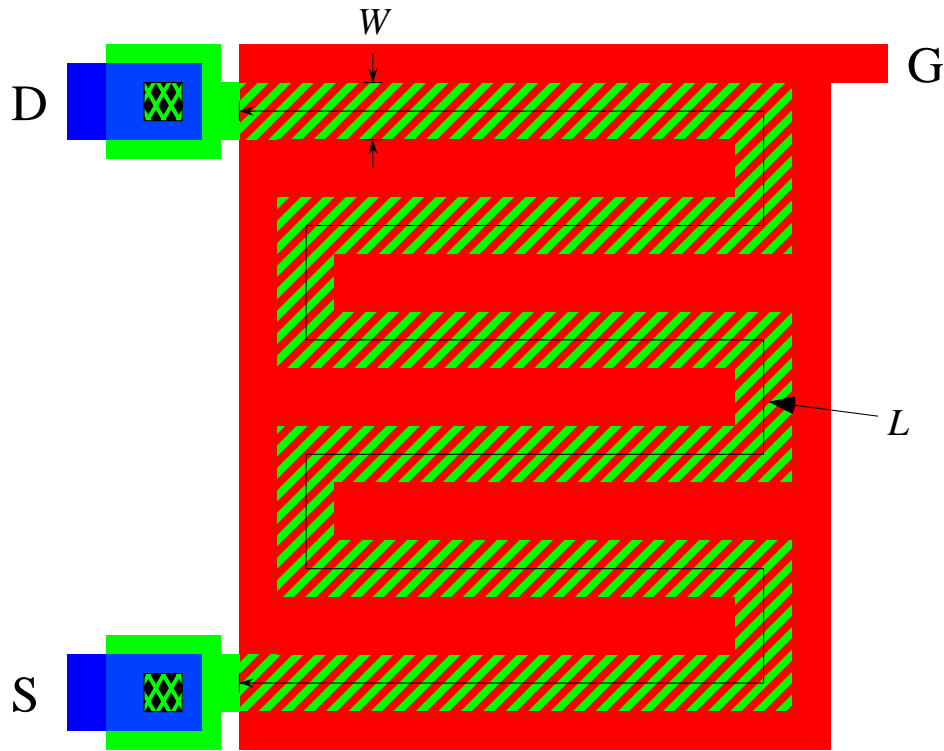
- ▶ Maximum W/L for a given C_D (drain inside).
- ▶ No channel edge \Rightarrow no edge effects.
- ▶ Circular shape best (uniform channel length, no corners), but not always allowed.

Very Wide MOS Transistors: Waffle Transistors



- ▶ Large W/L for a given area.
- ▶ Low parasitic source/drain capacitances.
- ▶ Low source, drain, and gate series resistances.
- ▶ Diagonal wires are useful, but not always allowed.

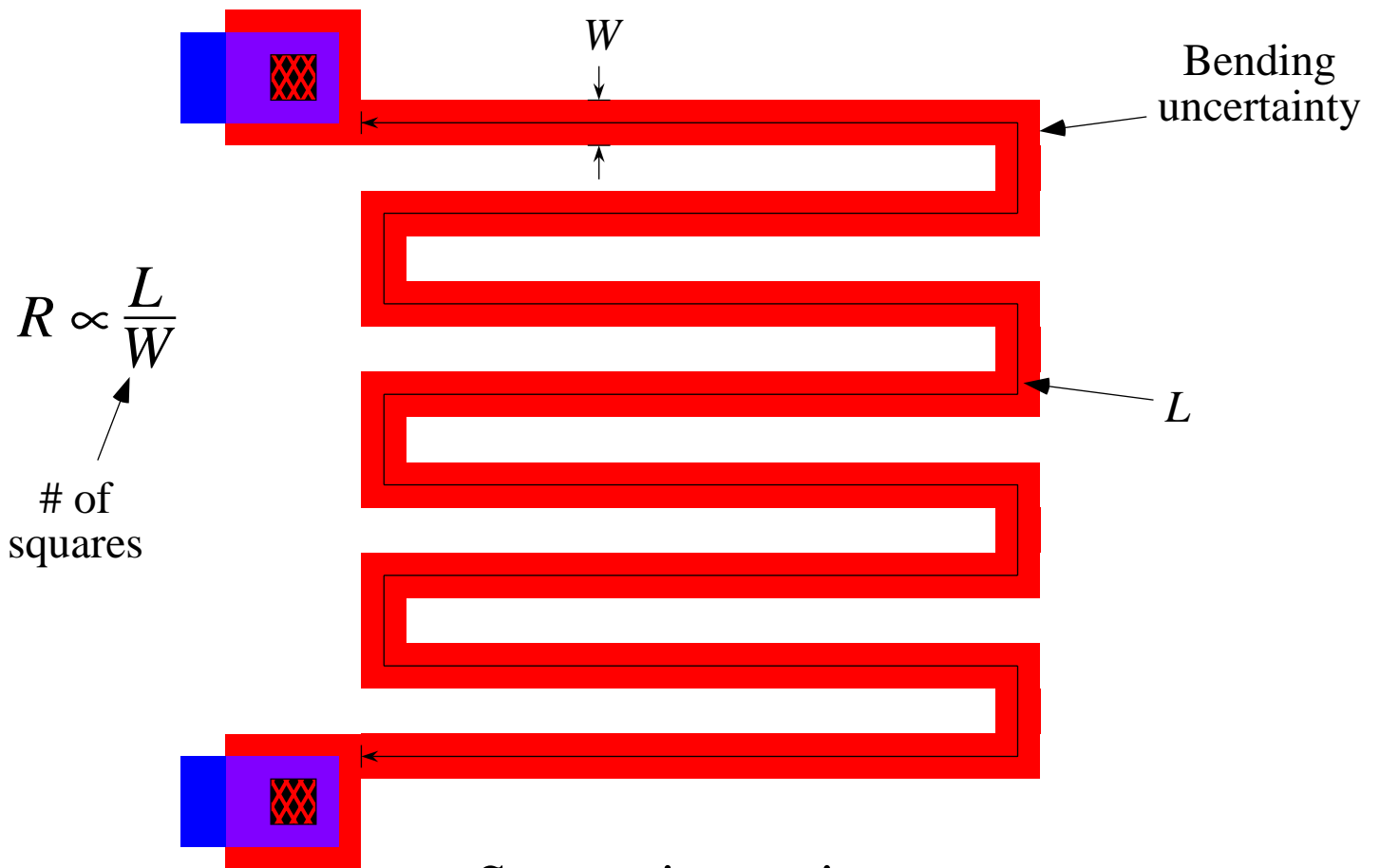
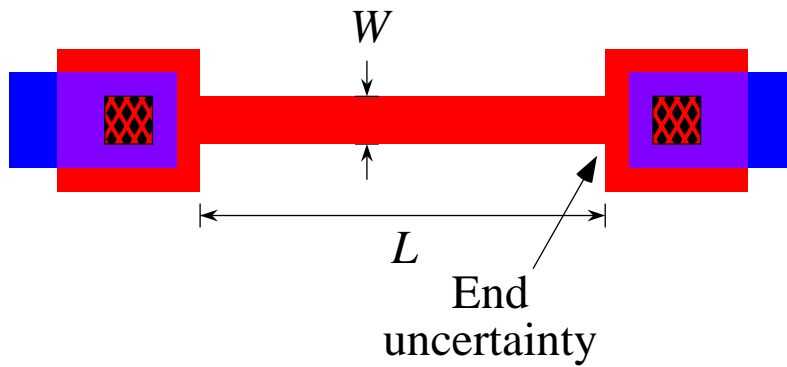
Very Long MOS Transistors: **Serpentine** Transistors



$$W \ll L$$

One large gate covers
the entire serpentine channel

Resistors

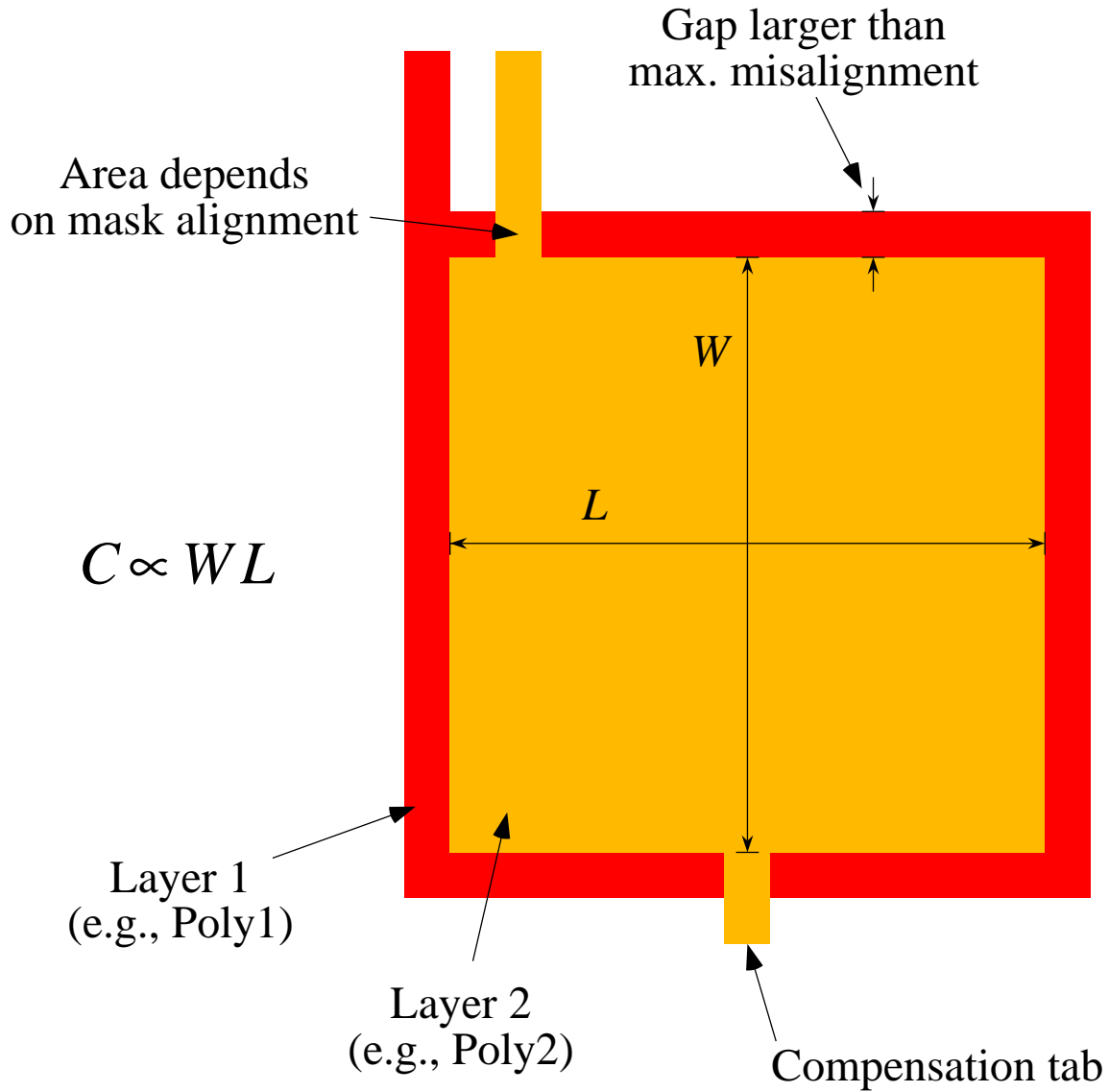


$$R \propto \frac{L}{W}$$

of squares

Serpentine resistor
large L/W

Capacitors

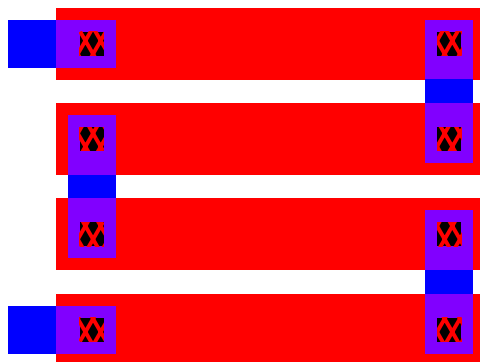


Control of Absolute Component Values

- ▶ Control device geometries by avoiding uncertainties.

Examples:

- Stacked vs serpentine MOS transistors
- Bending uncertainties in a resistor controlled by a low resistivity layer



- ▶ Avoid using minimum dimensions.

$$R = R_{\square} \frac{L}{W}$$

$$C = C_s WL$$

$$\frac{\Delta R}{R} = \underbrace{\frac{\Delta R_{\square}}{R_{\square}}}_{\text{indep. of } W \& L} + \underbrace{\frac{\Delta L}{L} - \frac{\Delta W}{W}}_{\text{minimize by making } W \gg W_{\min} \text{ and } L \gg L_{\min}}$$

$$\frac{\Delta C}{C} = \underbrace{\frac{\Delta C_s}{C_s}}_{\text{indep. of } W \& L} + \underbrace{\frac{\Delta L}{L} + \frac{\Delta W}{W}}_{\text{minimize by making } W \gg W_{\min} \text{ and } L \gg L_{\min}}$$

indep. of $W \& L$
~5-50%

minimize by making $W \gg W_{\min}$
and $L \gg L_{\min}$

indep. of $W \& L$
~5-50%

minimize by making $W \gg W_{\min}$
and $L \gg L_{\min}$

- ▶ Good circuit designs minimize reliance on absolute component values.

Layout for Device Matching

- ▶ Devices on the same die can match well (precision):

$$\frac{\Delta C}{C} \sim 0.1\% \quad \frac{\Delta R}{R} \sim 0.1\% \quad \frac{\Delta I_s}{I_s} \sim 1-10\%$$

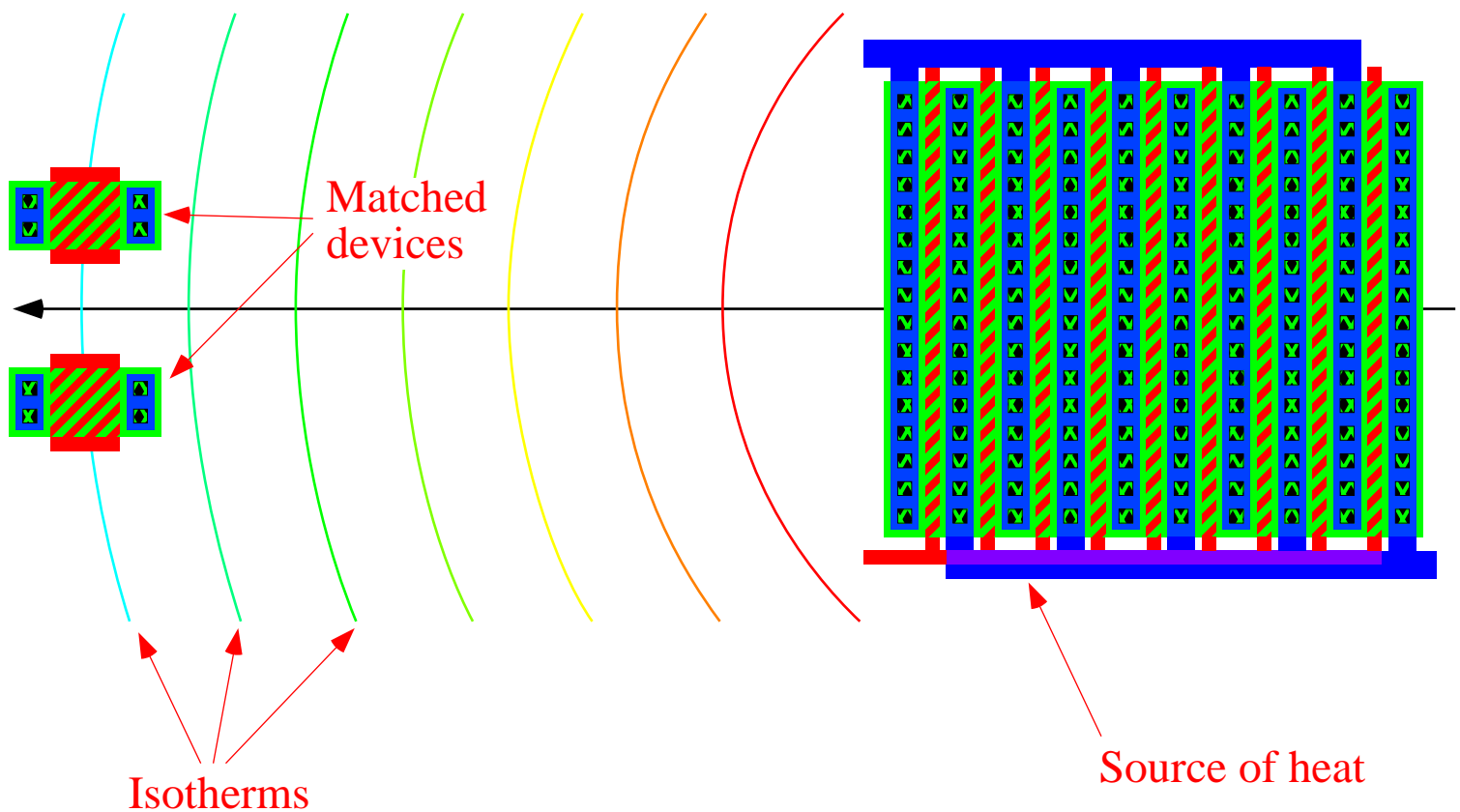
- ▶ For circuits characteristics (e.g., gains) that depend on **ratios** of component values,

Precise matching \Rightarrow Accurate characteristics

- ▶ To improve device matching, use devices with
 - Same temperature
 - Identical shape and size
 - Minimum spacing
 - Common centroid geometries
 - Same orientation
 - Same surroundings
 - Nonminimum size
- ▶ ***Caveat emptor!*** The relevance of each “rule” depends on particulars of the process and devices involved.

Matching: Same Temperature

- ▶ Not a serious problem if the total power dissipation on chip is low enough (e.g., subthreshold CMOS).
- ▶ Place devices symmetrically with respect to the source of heat along an isotherm:



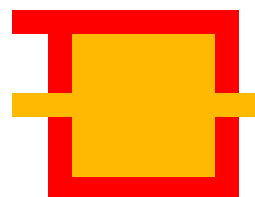
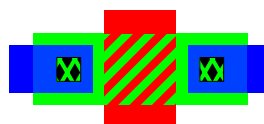
Matching: Identical Shape and Size

Resistor
(5 squares)

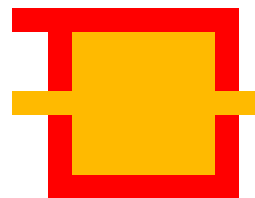
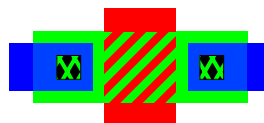
Transistor
($W/L = 1$)

Capacitor
(area A)

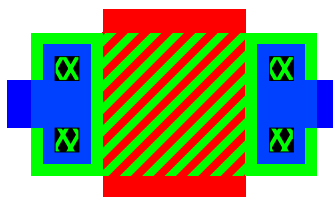
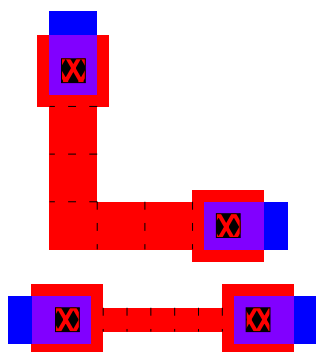
Ref.



Good



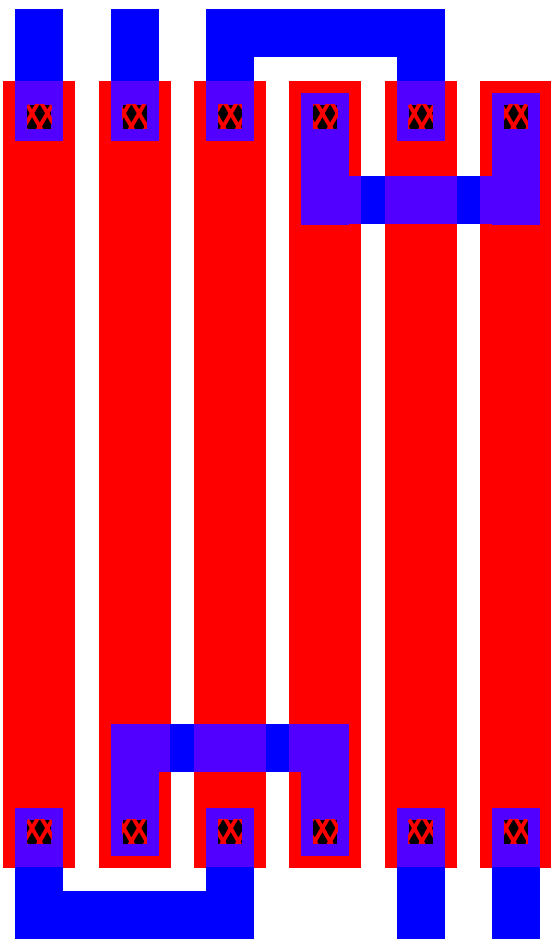
Bad



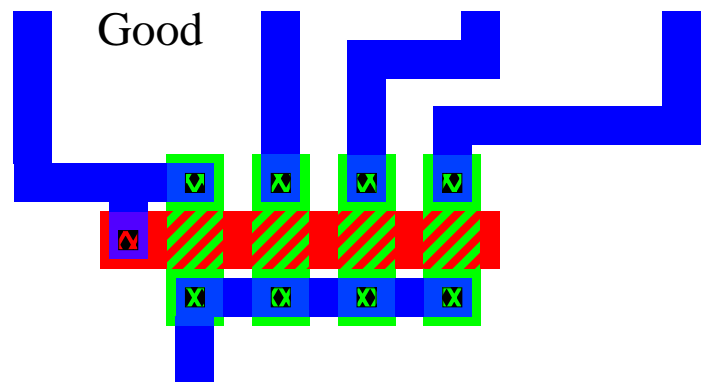
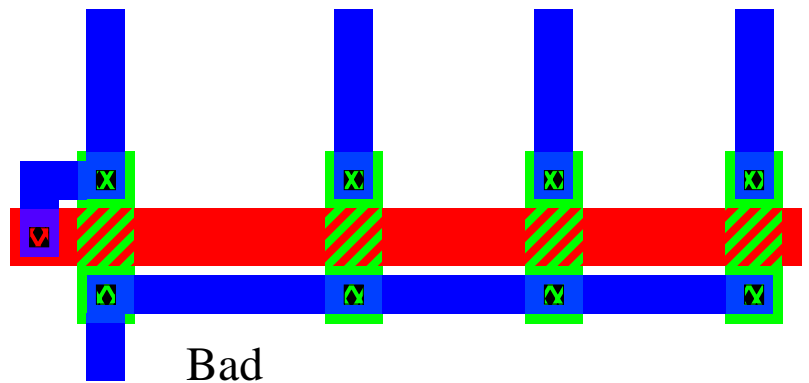
Matching: Minimum Distance

- ▶ Take advantage of spatial correlations.
- ▶ Place devices as close together as possible.
- ▶ Examples:

Matched Resistors

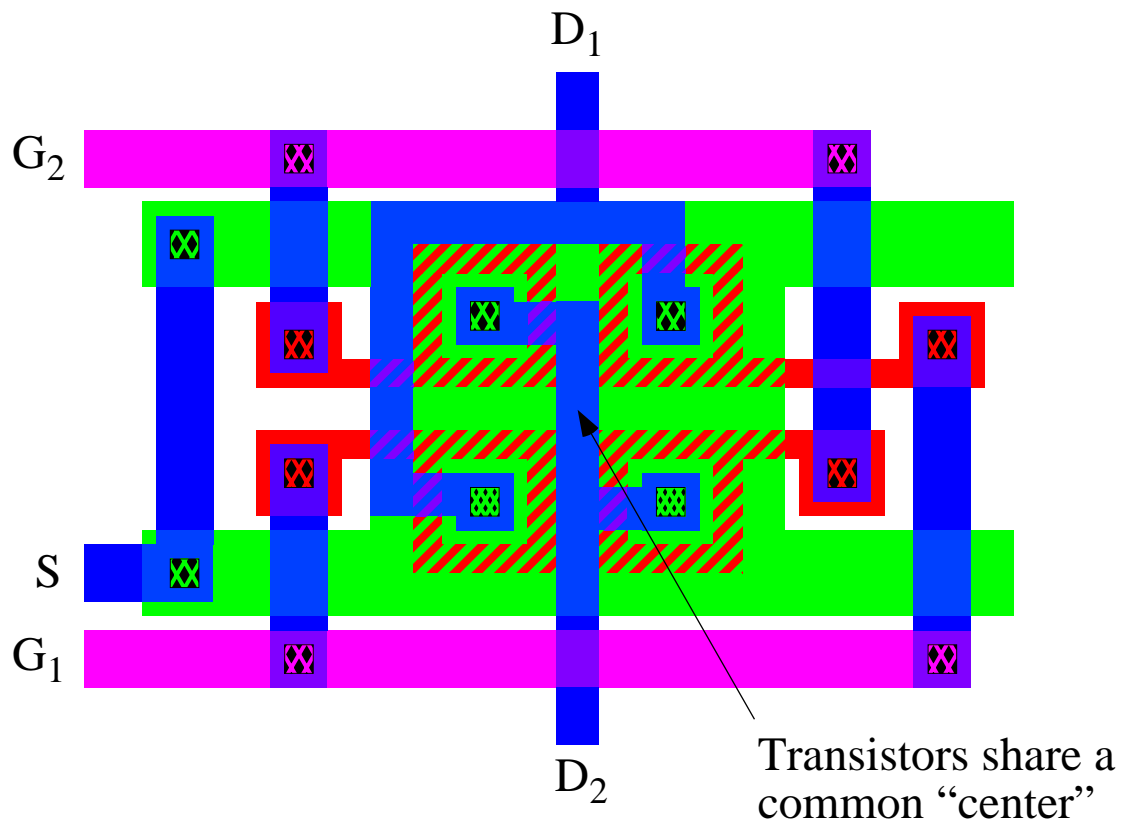


3-Output Current Mirror



Matching: Common Centroid

- ▶ Compensation of constant gradients
 - Temperature
 - Oxide thickness
 - Substrate Doping
- ▶ Example: Cross-coupled quad



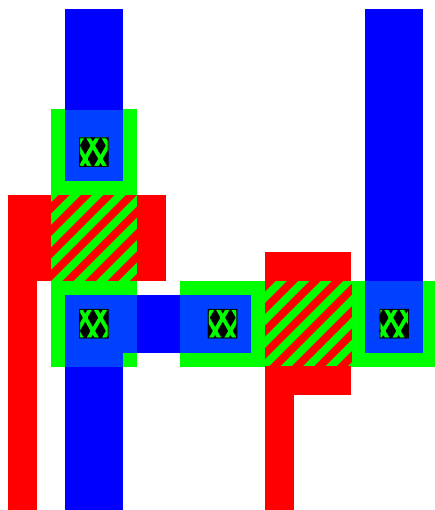
- ▶ Complicated layout \Rightarrow not practical for $> 2 \times 2$

Matching: Same Orientation

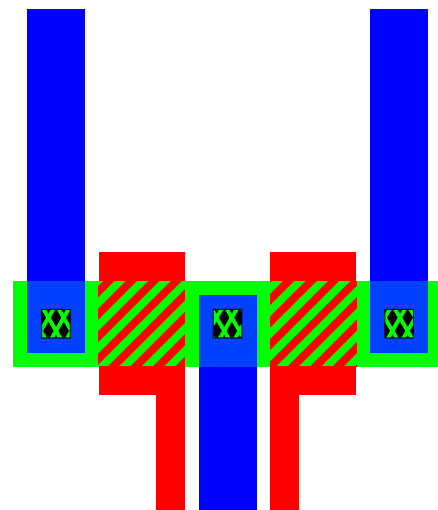
▶ Eliminate mismatch arising from:

- Anisotropic substrate
- Anisotropic process steps
- Packaging-induced stresses

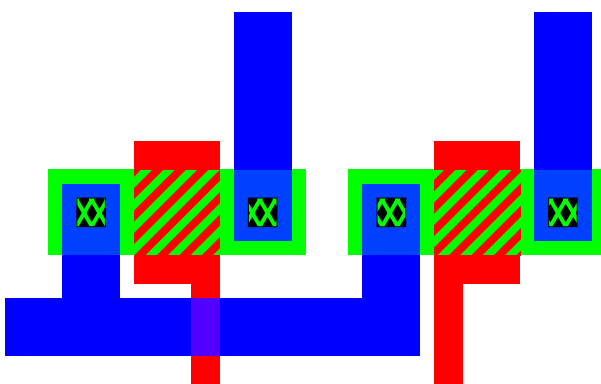
▶ Example: Differential Pair



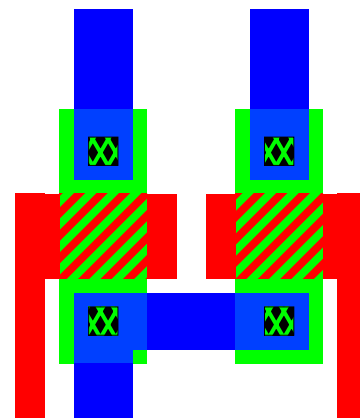
Ugly



Bad



Fair



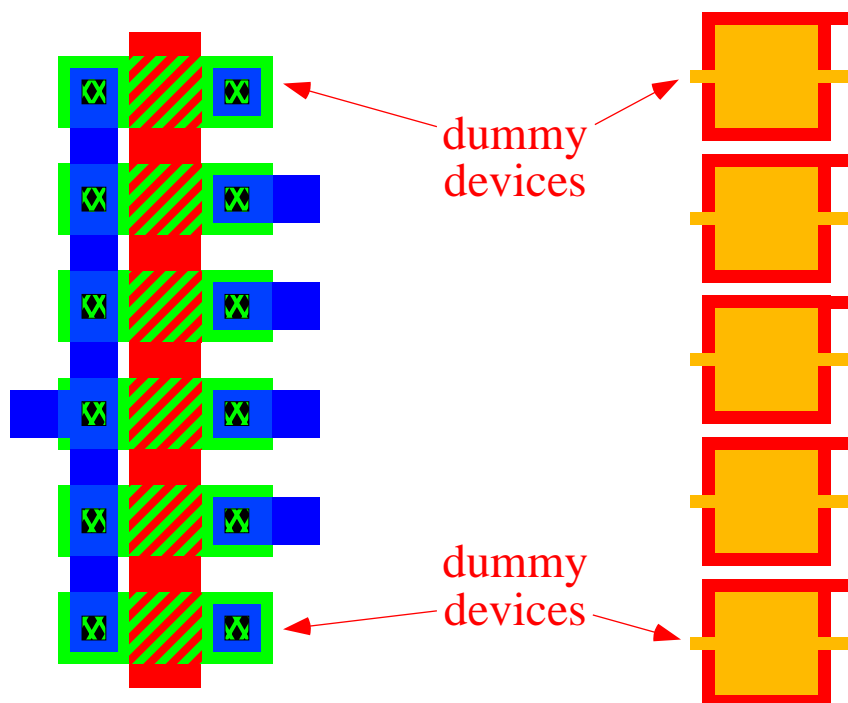
Good

Matching: Same Surroundings

- ▶ Reasons are not always clear. Possibilities include:
 - Fringing fields
 - Nonuniform lithography
 - Nonuniform etching during processing
- ▶ Use **dummy devices** to make all functional devices have the same surroundings.
- ▶ Examples:

Current Sources

Capacitors

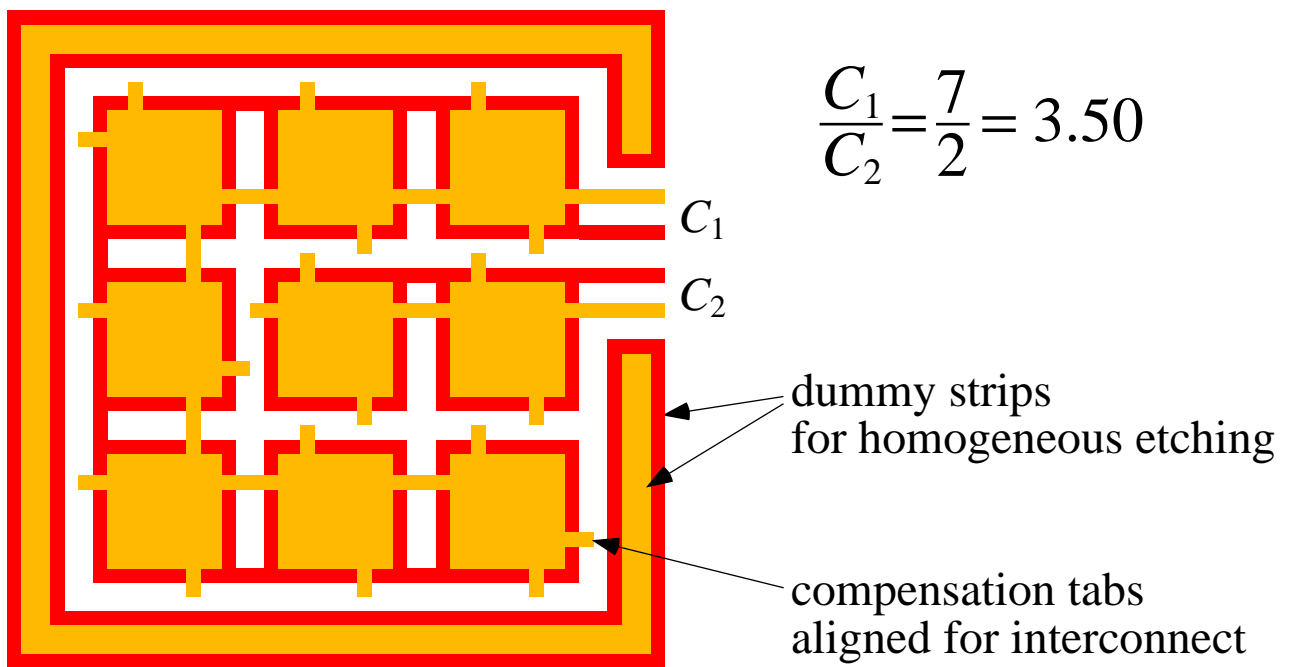


- ▶ Sometimes the surround can be simulated adequately with dummy strips.

Matching for Non-Unity Ratios

► For n/m ratios, use $n + m$ unit devices:

Example: Capacitors

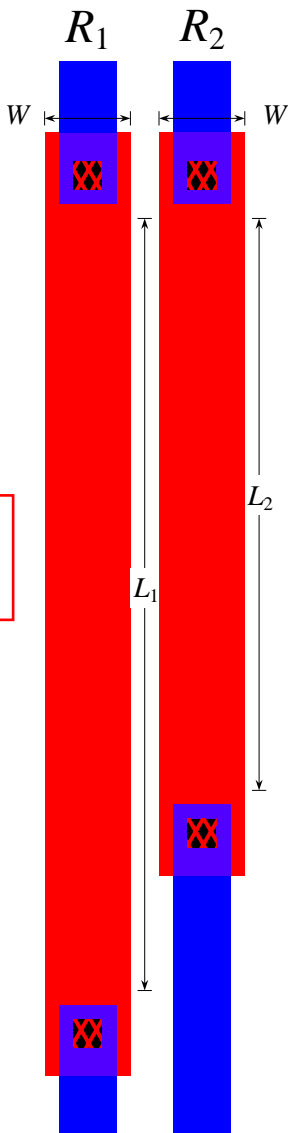


Matching for Non-Unity Ratios

► For arbitrary ratios, violate matching rules optimally.

Examples:

Resistors



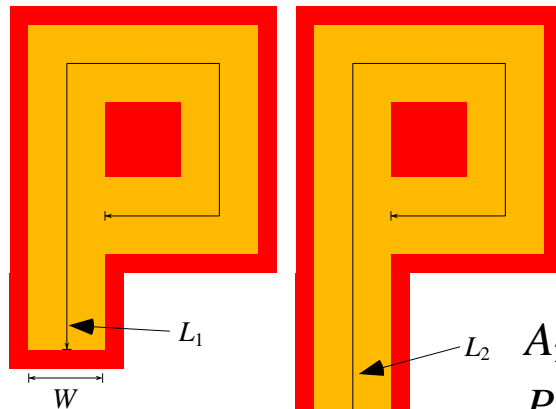
$$\frac{R_2}{R_1} = \frac{L_2}{L_1}$$

Same W ,
 $L_1 \gg L_{\min}$, $L_2 \gg L_{\min}$

Capacitors

C_1

C_2



$$A_1 = WL_1$$

$$P_1 = 2L_1$$

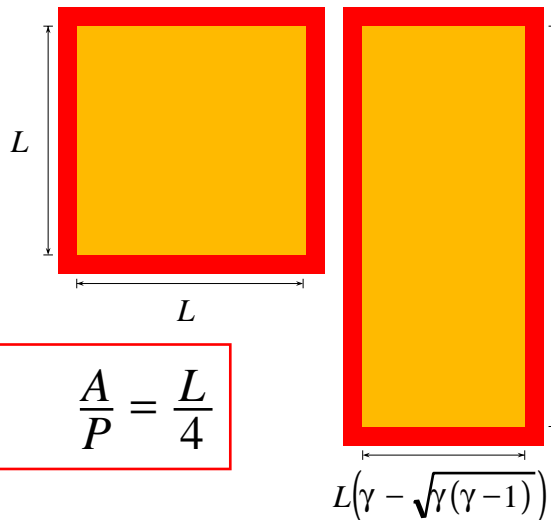
$$A_2 = WL_2$$

$$P_2 = 2L_2$$

$$\frac{C_2}{C_1} = \frac{L_2}{L_1} \quad \frac{A}{P} = \frac{W}{2}$$

C_1

C_2



$$A_1 = L^2$$

$$P_1 = 4L$$

$$L(\gamma + \sqrt{\gamma(\gamma-1)})$$

$$A_2 = \gamma L^2$$

$$P_2 = 4\gamma L$$

$$\frac{C_2}{C_1} = \gamma \quad \frac{A}{P} = \frac{L}{4}$$

Same area:perimeter ratio