Simple MOS Cascodes and Cascode Current Mirrors

2.1 Objectives

In this lab, you will examine the output current–voltage characteristics of a circuit configuration called a *cascode*. This term originally appeared in a January 1939 paper in the *Review of Scientific Instruments* by Hickman and Hunt entitled "On Electronic Voltage Stabilizers." They explained this term as a contraction of the phrase *casc*ade to cath*ode*, which is the terminal of a triode vacuum tube that is functionally analogous to the source of an MOS transistor. You will also consider the behavior of an improved current mirror made from a pair of MOS cascodes.

2.2 Prelab

The following prelab questions have been constructed to help you prepare to do the lab efficiently. Unless otherwise stated, you should assume that like transistors are matched and that the Early effect is negligible. Please complete these questions *before* you come to lab. While you may discuss the prelab questions with your lab partner or with other students in the class, each student in a lab group should complete the prelab assignment individually, so that you each understand the circuit that you will be testing and what you will be doing in the lab.

1. Consider the circuit shown in Fig. 2.1a comprising two nMOS transistors. If the voltage V_c, which is called the *cascode bias voltage*, is fixed, then this circuit configuration is called a *simple fixed-biased cascode*. We call the top transistor in this circuit the *cascode transistor* and we say that the transistor on the bottom *is cascoded by* the top transistor. Assuming that both transistors are saturated, use the EKV model to find an expression for the voltage on the intermediate node, V, in terms of V_c and V_{in} that is valid for all inversion levels.

2. If the cascode transistor were saturated, what would be the minimum allowable value of V_c to keep the bottom transistor saturated if V_{in} were (a) below threshold and (b) above threshold? If V_c were set at this minimum allowable value, what would be the minimum allowable value of V_{out} to keep both transistors saturated for each case?

3. Suppose that the cascode transistor were saturated and that V_c were fixed at some value that would be appropriate for an above-threshold value of V_{in}. Explain how I_{out} and V would change if V_{in} were swept from well below threshold to well above

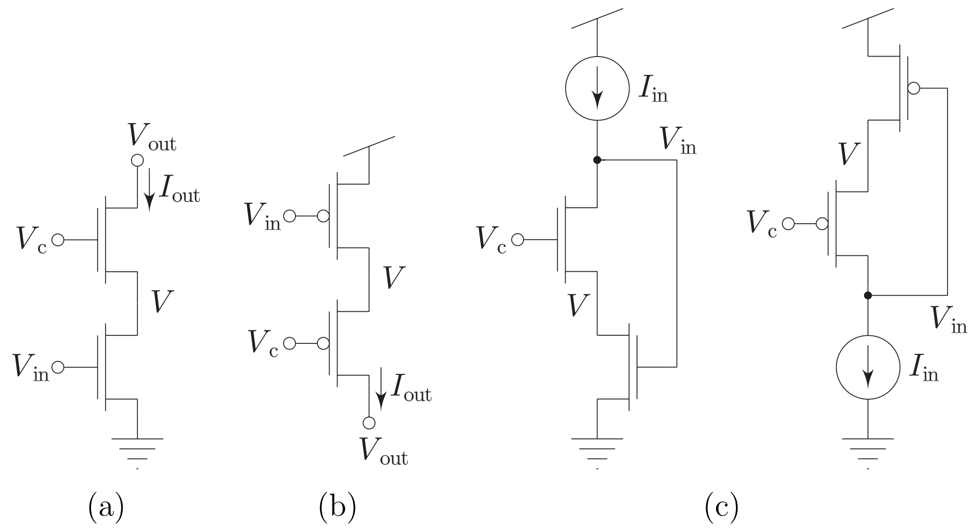

Figure 2.1: Simple fixed-bias (a) *n*MOS and (b) *p*MOS cascodes and (c) diode-connected cascodes.

threshold. In your explanation, be sure to comment on whether or not the bottom transistor remains saturated as V_{in} changes.

4. Consider the *p*MOS cascode, shown in Fig. 2.1b. In this case, the transistor on the bottom is the cascode transistor and the transistor on top is the transistor being cascoded. Answer the first three Prelab questions for the *p*MOS cascode.

5. Suppose that we connect a current source to the output of a cascode and connect V_{out} to V_{in}, as shown in Fig. 2.1c. This configuration is directly analogous to diode-connecting a single transistor. If V_c were fixed as we have been supposing, what determines the maximum input current that these circuits can accept?

6. Explain qualitatively how V_{in} and V would change in these circuits in response to I_{in}, if we were to sweep I_{in} slowly from deep in weak inversion to the maximum value that they can accept. In your explanation, be sure to comment whether or not each transistor would be saturated as I_{in} changes.

2.3 Experiments

You will be doing three experiments in this lab. In Experiment 1, you will examine how the intermediate node voltage behaves as a function of the input voltage and the cascode bias voltage. In Experiment 2, you will examine the output current–voltage characteristics of a cascode. In Experiment 3, you will examine a diode-connected cascode, which serves as the input side of a MOS cascode current mirror.

2.3.1 Experiment 1: Cascode Operating Point

In Capture CIS, construct an nMOS cascode. With the full power supply across the cascode, measure the intermediate node voltage, V, as a function of the cascode bias voltage, V_c, for three different values of V_{in}, one below threshold, one around threshold, and one above threshold. Does the value of the intermediate node voltage behave as you predicted in the prelab? In your report, include a plot showing V as a function of V_c for both values of V_{in}.

Next, with the full power supply across the cascode, measure V as a function of V_{in} for three values of V_c. Does the value of V depend on V_{in} as you predicted in the prelab? In your report, include a plot showing V as a function of V_{in} for both values of V_c.

Repeat this experiment for a pMOS cascode.

2.3.2 Experiment 2: Cascode Output Characteristics

Next, measure the output current of your nMOS cascode as a function of the output voltage for three different values of the cascode bias voltage for each of the three values of V_{in} that you chose in the first part of Experiment 1. Each cascode bias voltage that you choose should be higher than (i.e., further away from ground than) your input voltages. These output current–voltage characteristics of the cascode are analogous to drain characteristics of a single transistor. You will probably notice three distinct regions in each of these output characteristics, especially for the input voltage at or below threshold. In each of these regions, comment on whether or not each transistor in the cascode is saturated. For each value of V_{in}, include a plot showing I_{out} as a function of V_{out} for the three different values of V_c.

Repeat this experiment for a pMOS cascode.

2.3.3 Experiment 3: Cascode Current Mirror Input Stage

Reconfigure your cascode so that it is diode connected, as shown in Fig. 2.1c. For the values of the cascode bias voltage that you chose to use in Experiment 2, measure V_{in} as a function of I_{in} as you sweep I_{in} logarithmically from a weak-inversion level to a strong-inversion one. Does V_{in} remain relatively constant and then sharply increase during each of these sweeps? If so, does the input current at which this happens change with V_c? In your report, include a single plot showing V_{in} as a function of I_{in} for all sweeps.

Next, measure the intermediate node voltage, V, as a function of V_{in} over the range of values that V_{in} assumed as you swept I_{in} for each of the different values of V_c that you just used. Comment on whether or not each of the two transistors is saturated as V_{in} changes over this range. In your report, include a plot showing the voltage across each transistor as a function of V_{in} for all values of V_c that you used.

Repeat this experiment for a pMOS cascode.

2.4 Postlab

Consider the pair of cascodes, shown in Fig. 2.2a. If both cascode transistors were saturated, what relationship holds between V_1 and V_2 regardless of the value of V_{in}? What relationship

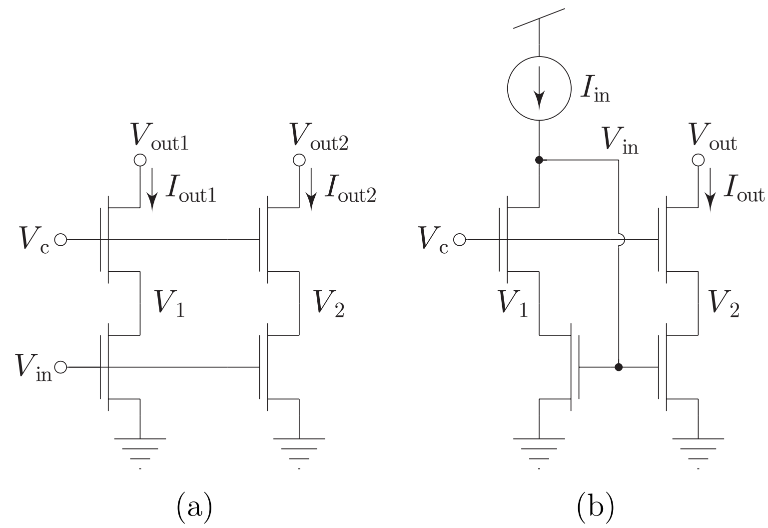

Figure 2.2: Development of a MOS cascode current mirror.

holds between I_{out1} and I_{out2} regardless of the value of V_{in}? Do the answers to these questions depend on whether or not the bottom transistors are saturated?

Suppose that we were to take the pair of cascodes of Fig. 2.2a, to source an input current into the output of the one on the left, and to make a diode connection above the cascode transistor on the left, as shown in Fig. 2.2b. This procedure is directly analogous to that by which we developed the simple current mirror. It should not be too surprising that this circuit is called a *cascode current mirror*. Suppose that V_c were fixed as we supposed in the Prelab section. What determines the maximum input current that this circuit can accept? If V_{out} were high enough to keep the output cascode transistor saturated, explain qualitatively how V_{in}, V_1, and V_2 would change in response to I_{in} if we were to sweep I_{in} slowly from deep in weak inversion to this maximum value. In your explanation, be sure to comment whether or not the input cascode transistor and the two bottom transistors would be saturated as I_{in} changes. Does this circuit function as a current mirror over this entire range of input currents? Explain your reasoning.